

**A SYSTEM ON A CHIP WITH MULTIPLE POWER
PLANES AND ASSOCIATE POWER MANAGEMENT METHODS**

ABSTRACT OF THE DISCLOSURE

A system-on-a-chip includes a first and second power planes for respectively powering core logic and analog portions of the system. Clock generation circuitry is included for generating clocks for clocking operations of selected circuits of the system on a chip in response to a signal generated by an oscillator. Power control circuitry switches off power to the first and second power planes in a first mode, with the oscillator being enabled. In a second mode, the power control circuitry disables the clock generation circuitry and switches power to the first and second power planes, the oscillator being enabled.

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